UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,564	03/30/2004	Bertrand Bertrand	02RO42254500	4127

27975 7590 11/02/2006

ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,564	BERTRAND ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/21/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,13,16-23,26-33 and 36-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,13,16-23,26-33 and 36-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 9/21/06. The rejection in previous office action is maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 12, 13, 16-23, 26-33 and 36-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Naura (USP 6127898).

As to claim 12, Naura discloses in figure 5 a comparator (circuit on the right of capacitor C) with two thresholds comprising: a two-threshold latch including an input (E) and an output (output of 3) respectively forming an input and an output of the comparator, and including a first node (C) between a first power supply terminal (Vdd) and the output of the comparator; and a first negative feedback loop (T5, T7', T8) acting on the first node for setting a first threshold of the comparator as a function of a first power supply potential (Vdd or ground) applied to the first power supply terminal, and as a function of a first reference potential (Vref1), wherein the first threshold is an upper triggering threshold (Vb, col. 3, lines 36-50 teaches that the transistors in upper circuit turn on when the voltage at the input terminal E is lower than Vb. Therefore, Vb can be considered as upper triggering circuit), and the first reference potential (1 volt, col. 5, lines 34-36) is less than or equal to the first power supply potential, which is positive, and wherein a difference between the first power supply potential and the first reference potential is positive (figure 6 shows that VDD is equal to 5 volts; therefore, VDD – Vref1 is about 4 volts which is positive) and increases as a function of the first power supply potential to limit an

increase in the first threshold when the first power supply potential increases (Col. 5, lines 30-40, teaches Vref is constant. Therefore, when Vdd increases, the different between Vdd and Vref1 also increases).

As to claim 13, figure 5 shows that the two-threshold latch further includes a second node (D) between a second power supply terminal and the output of the comparator; and further comprising a second negative feedback loop (T6, T9', T10) for setting a second threshold of the comparator as a function of a second power supply potential (ground or Vdd) applied to the second power supply terminal, and as a function of a second reference potential (Vref2).

As to claim 16, figure 5 shows that the second threshold is a lower threshold, and the second reference potential is greater than or equal to the second power supply potential, which is ground.

As to claim 17, figure 5 shows that the first negative feedback loop comprises first and second transistors (T5, T7') each comprising a source, a drain and a gate, with the source of the first transistor being connected to the first node, the gate of the first transistor being connected to the source of the second transistor, the gate of the second transistor being connected to the output of the comparator, the first power supply potential (ground) being applied to the drain of the first transistor, and the first reference potential being applied to the drain of said second transistor.

As to claim 18, figure 5 shows that the first negative feedback loop further comprises a third transistor (T8) comprising a drain connected to the gate of the first transistor, a gate connected to the output of the comparator, and a source connected to the second power supply potential (Vdd).

As to claim 19, figure 5 shows the second negative feedback loop comprises fourth and fifth transistors (T6, T9') each comprising a source, a drain and a gate, with the source of the

fourth transistor being connected to the second node, the gate of the fourth transistor being connected to the source of the fifth transistor, the gate of the fifth transistor being connected to the output of the comparator, the second power supply potential being applied to the drain of the fourth transistor, and the second reference potential being applied to the drain of the fifth transistor.

As to claim 20, figure 5 shows that the second negative feedback loop further comprises a sixth transistor (T10) comprising a drain connected to the gate of the fourth transistor, a gate connected to the output of the comparator, and a source connected to the first power supply potential.

As to claim 21, figure 5 shows that the two-threshold latch comprises a plurality of transistors (T1-T4) series-connected between the first power supply terminal and a second power supply terminal, the plurality of transistors each comprising a gate connected together and to the input of the two-threshold latch, the plurality of transistors including seventh and eight transistors (T1, T2) having a first type of conductivity, and ninth and tenth transistors having a second type of conductivity (T3, T4).

As to claim 22, figure 5 shows that the eight and ninth transistors each comprises a drain connected together; and wherein the two-threshold latch further comprises an inverter (3) connected between the drain of the eighth and ninth transistors and the output of the comparator.

Claims 23, 26-33 and 36-42 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

Response to Arguments

3. Applicant's arguments have been fully considered but they are not persuasive. Col. 3, lines 36-66, teaches that the upper transistors turn of when VE is lower than Vb, and the lower

transistors turn on when VE is higher than Vh. Thus, Vb is triggering threshold of the upper transistors and Vh is the triggering threshold of the lower transistors. Therefore, Vb can be considered as the upper triggering threshold, and Vh can be considered as the lower threshold.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

October 26, 2006